REMARKS

Claims 1-10 are pending in the present application. Claims 1-10 are rejected. No new matter has been entered.

Claim Rejections - 35 U.S.C. §103

Claims 1-3 and 5-8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Corvasce et al. US 6,300,654 B1 in combination with Sasaki et al. US 6,444,099 B1 and Matsuura et al US 6,964,873 B2.

The Examiner asserts that it would have been obvious to provide the method in Corvasce et al. with the Ti sputtering while keeping substrate temperature higher than room temperature and lower than 200 °C as taught by Sasaki et al. or Matsuura et al. because the Ti sputtering of Sasaki et al./Matsuura et al. would provide the method of Corvasce et al. with prevention of "a problem with collimation sputtering is that sputter particles accumulate on the collimator portion, and the resulting loss material decreases the deposition rate" (Sasaki et al. col. 2, lines 5-10).

Claims 4 and 10 are rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Corvasce et al. with Sasaki et al. and Matsuura et al. as applied to claims 1-3 and 5-8 above, and further in view of Ohwaki et al., "Preferred Orientation in Ti Film Sputter-Deposited on SiO_2 Glass: The Role of Water Chemisorption on the Substrate", Jpn. J. Appl. Phys., Vol. 36 (1997) pp L154-L157.

The Examiner concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of Corvasce et al. with the conditions of

Ohwaki et al. or Matsuura et al. because the conditions of Ohwaki et al. or Matsuura et al. would provide the ferroelectric capacitor of Corvasce et al. with the Ti (002) preferred orientation for the reliability of the electrode (Ohwaki et al.) and with better adhesion (Matsuura et al.)

Claim 9 is rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Corvasce et al. with Sasaki et al. and Matsuura et al. as applied to claims 1-3 and 5-8 above, and further in view of Noguchi et al., US 6,716,749.

The Examiner concludes that it would have been obvious to one of ordinary skill in the art to provide the process of the combination with NH_3 plasma nitride before the lower layer of the lower-electrode conductive film is formed because the plasma nitride would improve the surface of the insulating film as taught by Noguchi et al.

The Examiner notes Applicants' argument that with the change in temperature limitation from 300 °C down to 200 °C there are unexpected results associated with the present invention. The Examiner reasserts that choice of temperature or partial pressures of elements would have been a matter of routine optimization. The Examiner insists that one of ordinary skill in the art would have been led to the claimed temperature of higher than room temperature and lower than 200 °C while forming a Ti lower layer through the teaching of Sasaki et al. and Matsuura et al. to achieve desired deposition and reaction rates as same as in the instant invention.

Applicants respectfully disagree with the above rejections, and submit that the claimed parameters are not directly taught by the combination of the cited reference, and the claimed

parameters provide unexpected results over what might have been expected based on the cited combination of references.

The Examiner asserts that it would have been obvious to provide the method in Corvasce et al. with the Ti sputtering while keeping substrate temperature higher than room temperature and lower than 200 °C as taught by Sasaki et al. or Matsuura et al. because the Ti sputtering of Sasaki et al./Matsuura et al. would provide the method of Corvasce et al. with prevention of "a problem with collimation sputtering is that sputter particles accumulate on the collimator portion, and the resulting loss material decreases the deposition rate" (Sasaki et al. col. 2, lines 5-10).

The present claims recite that the substrate of the present invention is maintained at "higher than room temperature and lower than 200 °C". Applicants submit that such temperature range provides results that would have been unexpected in light of the suggested range of 50 °C to 500 °C of Sasaki et al.

Applicants note that Fig. 3 of the present invention shows the drop off in degree of orientation in the (222) direction of a Pt film formed on the Ti film when the substrate is formed above 150 °C. The extrapolation of the graph of Fig. 3 shows the steepened drop off above 200 °C. Such drop off would not have been expected in light of Sasaki et al., which does not differentiate between 50 °C and 500 °C, or any temperature therebetween.

Applicants have previous submitted that even if the cited references were properly combined and the obviousness rejection had merit, the recited temperature range produces unexpected results, as noted in Figs. 2 and 3.

Applicants submit herewith additional results that indicate that the claimed range of "higher than room temperature and lower than 200 °C" provides unexpected results over temperatures in the range of 50 °C to 500 °C of Sasaki et al. but outside the claimed range.

The reference chart attached hereto shows an example of data retention characteristics in the FeRAMs to which the present invention is applied, and is the data obtained as a result of the durability (reliability) test carried out by the inventor after the filing of this application. In the illustrated graph, the "data retention characteristics" represent a ratio (%) of the number of chips from which data could be normally read, to the total number of chips (which normally function) into which data were written.

The durability test was carried out by the following process:

First, with respect to all of the chips (approximately 1000 chip) on the wafer which underwent all of the semiconductor processes, testing whether or not the individual chips normally function as an electric circuit, respectively; then writing data into chips which normally functioned among them; leaving the wafer (chips into which data were written) at approximately 200°C in five or six hours as it is, to thereby deteriorate the written data; and with respect to the chips into which data were written, testing whether or not the data could be normally read.

This graph exhibits a tendency similar to the characteristics (Ti (002)) intensity relative to the substrate temperature) shown in FIG. 2, and shows that the data retention characteristics can be improved by keeping the substrate temperature at a temperature higher than room temperature and lower than 200 °C.

These results (data retention characteristics in the FeRAMs) are not referred to, suggested or expected in any of the cited references, and accordingly, even if the teachings of respective references are combined, it would not have been obvious to one of ordinary skill in the art to easily form a high reliability ferroelectric capacitor as in the claimed invention. Applicants will submit such data in the form of an Inventor's Declaration shortly.

Sasaki teaches that its heater controls the temperature of the substrate 50 over a range from room temperature to about 500 °C. However, even if this were a suggestion to use any temperature in the range, Applicants submit that the present specification includes unexpectedly superior results in the range of room temperature to 200 °C., especially as indicated by the sharp drop off indicated in Fig. 3 of the specification.

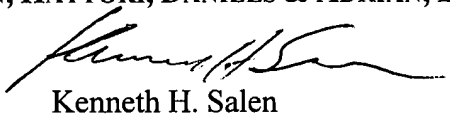
In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



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Enclosures: Reference chart showing data retention characteristics at various temperatures